UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,283	07/31/2001	Duane E. Galbi	00CXT0725N-1	2490

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EXAMINER
SCHEIBEL, ROBERT C

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	09/919,283	GALBI ET AL.
Office Action Summary	Examiner	Art Unit
	Robert C. Scheibel	2666

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 January 2005</u>.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-21* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All   b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).
   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 11/24/2004 has been entered.

2.   Applicant's arguments, see page 8, filed 11/24/2004, with respect to the rejection of

claims 1-21 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore,

the rejection has been withdrawn. However, upon further consideration, a new ground of

rejection is made in view of U.S. Patent 6,021,132 to Muller et al. Examiner notes that claim 10

was indicated as having allowable subject matter in the previous office action. However, it has

been determined in view of the broad language of this claim that Muller clearly discloses the

limitations of this claim.

Specification

3.   The disclosure is objected to because of the following informalities: the status of several

applications listed in the specification need to be updated. For example, the status of the

following applications listed on page 1 should be updated as indicated:

- 09/639,915: current status is "now pending";

- 09/640,258: current status is "now patent number 6,754,223";

- 09/640,231: current status is "now patent number 6,804,239".

Also, the following applications listed on page 3 should be updated as indicated:

- 09/639,966: current status is "now patent number 6,760,337";

- 09/640,231: current status is "now patent number 6,804,239";

- 09/640,258: current status is "now patent number 6,754,223".

These applications are also listed on page 7 along with 09/640,260, which is still pending.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims **1-21** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent

6,021,132 to Muller et al.

Regarding claims **1 and 21**, Muller discloses An integrated circuit for processing events

related to communication packets (switching element 100 of Figure 2; see also lines 38-44 of

column 9 for a description of the single integrated circuit preferred embodiment), said integrated

circuit comprising: a core processor (network interface 205 of Figure 2) configured to execute

software to process a series of communication packets (see lines 48-65 of column 5), the

processing of each packet being an event and having associated data and context information

(see lines 44-51 of column 8); and a co-processor (Shared Memory Manager 220 of Figure 2, the

details of which are illustrated in Figures 3B and 4) comprising a plurality of state information

buffers (the elements in the tag array 420 and counter array 430 of pointer RAM 320 in Figures

3B and 4) for storing state information where the state information comprises at least one of the

following: a data buffer pointer (lines 2-7 of column 10), a context pointer (lines 2-7 of column

10 and lines 44-51 of column 8), context-validity bit, requester indicator (buffer ownership as

discussed in lines 40-41 of column 6), port status, a channel descriptor loaded indicator; the state

information is associated with events wherein each of said state information buffers having an in-

use counter (the count stored in the count array 430 described throughout, including the passage

from line 66 of column 9 through line 2 of column 10) indicating the number of events

associated with the contents of said buffer (the processing done for transmitting out each port is a

separate event).

Muller similarly discloses the limitations of claim **10**. Claim 10 has the additional

limitation that data can be passed from one event to another event by changing the data in one of

said state information buffers. This is disclosed by the transfer of buffer ownership discussed in

Muller in columns 11 and 12. For example, lines 34-36 of column 11 specify that the count field

is updated as part of the ownership transfer. Additionally, it is clear that this count field is

associated with both the context and data discussed in lines 44-51 of column 8 as both are

required for the output processing event performed to send the packet out the correct port.

Regarding claim **11**, Muller discloses a method of processing events related to

communication packets in an integrated circuit (switching element 100 of Figure 2; see also lines

38-44 of column 9 for a description of the single integrated circuit preferred embodiment) which

includes a core processor (network interface 205 of Figure 2) and a co-processor (Shared

Memory Manager 220 of Figure 2, the details of which are illustrated in Figures 3B and 4)

having a state information buffer for storing state information (the elements in the tag array 420

and counter array 430 of pointer RAM 320 in Figures 3B and 4) where the state information

comprises at lease one of the following: a data buffer pointer (lines 2-7 of column 10), a context

pointer (lines 2-7 of column 10 and lines 44-51 of column 8), context-validity bit, requester

indicator (buffer ownership as discussed in lines 40-41 of column 6), port status, a channel

descriptor loaded indicator, the state information for an event is stored separate from the data

associated with said event (the data is stored in the shared memory, while the state information is

inside the co-processor (Shared Memory Manager 220)), said state information buffer having an

associated in-use counter (the count stored in the count array 430 described throughout,

including the passage from line 66 of column 9 through line 2 of column 10), the method

comprising: incrementing the in-use counter associated with said state information buffer when

an event is associated with said state information buffer (lines 34-36 of column 11 and line 61 of

column 11 through line 2 of column 12); and decrementing the in-use counter of said state

information buffer when said event associated with said buffer is finished (lines 22-29 of column

7 and lines 49-53 of column 12).

Regarding claim **16**, Muller discloses an integrated circuit (switching element 100 of

Figure 2; see also lines 38-44 of column 9 for a description of the single integrated circuit

preferred embodiment) for processing events associated with communication packets which

includes a core processor (network interface 205 of Figure 2) and a co-processor (Shared

Memory Manager 220 of Figure 2, the details of which are illustrated in Figures 3B and 4), the

improvement which comprises, separate buffers for data and state information (the data is stored

in the shared memory, while the state information is inside the co-processor (Shared Memory

Manager 220)) and in-use counters for all of said buffers (the count stored in the count array 430

described throughout, including the passage from line 66 of column 9 through line 2 of column 10), whereby the contents of a data can be passed from one event to another event (the transfer of buffer ownership discussed in Muller in columns 11 and 12. For example, lines 34-36 of column 11 specify that the count field is updated as part of the ownership transfer), each of said events having state information in a separate state information buffer where the state information comprises at least one of the following: a data buffer pointer (lines 2-7 of column 10), a context pointer (lines 2-7 of column 10 and lines 44-51 of column 8), context-validity bit, requester indicator (buffer ownership as discussed in lines 40-41 of column 6), port status, a channel descriptor loaded indicator.

Regarding claims **2, 4, 7, 14, and 17**, Muller discloses the limitations of a plurality of data buffers and a plurality of context buffers in lines 37-51 of column 8. The control information is the context buffers.

Regarding claims **3, 5, 8, 9, and 18**, Muller discloses the in-use counters associated with the data and/or context buffers in the count stored in the count array 430 described throughout, including the passage from line 66 of column 9 through line 2 of column 10. These counts are clearly associated with the data and the context as they indicate how many events (or output ports) are associated with the data and control information in the buffers.

Regarding claim **6**, Muller discloses the in-use counter associated with the data buffers in the count stored in the count array 430 described throughout, including the passage from line 66 of column 9 through line 2 of column 10. These counts are clearly associated with the data as they indicate how many events (or output ports) are associated with the data information in the buffers. The limitation that data can be transferred from one event to another event by changing

information in a data buffer is disclosed in the transfer of buffer ownership discussed in Muller

in columns 11 and 12. For example, lines 34-36 of column 11 specify that the count field is

updated as part of the ownership transfer.

Regarding claim **12**, Muller discloses the limitation that the integrated circuit comprises a

plurality of state information buffers in the elements in the tag array 420 and counter array 430

of pointer RAM 320 in Figures 3B and 4.

Regarding claims **13 and 15**, Muller discloses the limitation that said integrated circuit

comprises a context buffer (see lines 44-51 of column 8) and an in-use counter (the count stored

in the count array 430 described throughout, including the passage from line 66 of column 9

through line 2 of column 10; this counter is associated with the context information (control

information) in that it represents how many events (output port processing) are associated with

the context information) for said context information buffer and the method further comprises:

incrementing the in-use counter associated with said context buffer when an event is associated

with said context buffer (lines 34-36 of column 11 and line 61 of column 11 through line 2 of

column 12); and decrementing the in-use counter of said context buffer when said events

associated with said context buffer is finished (lines 22-29 of column 7 and lines 49-53 of

column 12). Muller discloses the additional limitation of claim 15 of the data only buffer in the

buffers used to store the packet data (lines 41-51 of column 8, for example).

Regarding claim **19**, Muller discloses the limitation of a plurality of data buffers (the

buffers used to store the packet data (lines 41-51 of column 8, for example)) and a plurality of

state information buffers (the elements in the tag array 420 and counter array 430 of pointer

RAM 320 in Figures 3B and 4).

Regarding claim **20**, Muller discloses a plurality of data buffers (the buffers used to store the packet data (lines 41-51 of column 8, for example)), a plurality of state information buffers (the elements in the tag array 420 and counter array 430 of pointer RAM 320 in Figures 3B and 4) and a plurality of context information buffers (see lines 44-51 of column 8), each of said plurality of data buffers and each of said plurality of state information buffers and each of said plurality of context buffers having an in-use counter (the count stored in the count array 430 described throughout, including the passage from line 66 of column 9 through line 2 of column 10) which is incremented when an event is associated with one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffers (lines 34-36 of column 11 and line 61 of column 11 through line 2 of column 12) and decremented when an event is finished utilizing one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffer (lines 22-29 of column 7 and lines 49-53 of column 12).

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,667,978 to Delp et al, U.S. Patent 6,625,986 to Narad et al and 6,157,955 to Narad et al disclose state information buffers similar to those now claimed with the newly amended limitations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Monday and Thursday from 6:30-5:00 Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RCS　3-17-05

Robert C. Scheibel
Examiner
Art Unit 2666

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